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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/916,598
Filing Date: July 26, 2001
Appellant(s): VENKITAKRISHNAN ET AL.

John P. Wagner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/23/06 appealing from the Office action mailed 7/25/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 6,587,926 B2	ARIMILLI	07-2003
US 6,571,322 B2	ARIMILLI-2	05-2003
US 6,560682 B1	MILLER	05-2003
US 6,418460 B1	BITAR	07-2002
US 2002/0184546 A1	SHERBURNE	12-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. *Claims 1-4, 7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli (US 6587926).*

Regarding claim 1, Arimilli discloses the processor units (e.g., Figure 1, "102"), cache units (e.g., Figure 1, "108"), embedded RAM (e.g., Figure 1, "114"), a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processors and the embedded RAM unit (e.g., col. 2, lines 1-5).

Regarding claim 2, Arimilli also discloses an input output unit coupled to the bus to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 3, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 4, Arimilli also discloses the bus is configured to transfer an entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 7, Arimilli also discloses support of a symmetric multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 9, Arimilli also discloses the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit (e.g., col. 7, lines 54-56).

Claim Rejections - 35 USC § 103

2. *Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Arimilli (US 6571322, hereinafter Arimilli-2).*

Regarding claim 5, Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli at the time the invention was made to obtain the claimed invention.

3. *Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of standard practice of memory implementation, as further evidenced by Miller (6560682).*

Regarding claim 6, Arimilli discloses an embedded RAM core, but fails to disclose the detail of using DRAM to implement memory; however the examiner takes Official Notice that the use of a DRAM core is standard embodiment of a RAM memory. This is further evidenced by Miller. Miller discloses the embedded DRAM core (e.g., col. 5, lines 7-10). It would be obvious to combine the DRAM implementation of memory with Arimilli because the embedded DRAM core is a standard means to implement a RAM unit. Therefore it would be obvious to one of ordinary skill in the art to combine a standard memory embodiment with the disclosure of Arimilli.

4. *Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of standard embodiment of a processor, as further evidenced by Bitar (US 6418460).*

Regarding claim 8, Arimilli neglects to disclose implementational details of a particular processor core; however the Examiner takes Official Notice that MIPS architecture is a standard processor and is well-known for its implementation in symmetric multiprocessing systems, such as in the system of Arimilli. This is further evidenced by Bitar. Bitar discloses the multi-processor units are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line

39; and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious to combine Arimilli with the standard MIPS architecture, because the use of MIPS architecture is widely known in the implementation of symmetric multiprocessing systems such as the system of Arimilli. Therefore at the time the invention was made, it would be obvious to a person of ordinary skill in the art to combine the MIPS architecture, as evidenced by Bitar, with Arimilli to obtain the claimed invention.

5. *Claims 10-13, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of the standard practice of integrating circuits, as further evidenced by Sherburne (2002/0184546).*

Regarding claim 10, Arimilli discloses a power supply; a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the processor units; an embedded RAM unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die; however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages

of portability, power consumption, and so forth. This is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices to obtain the advantages of decreased size and weight (e.g., paragraph [0002]). It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which included multiprocessing systems with cache and embedded memory. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

Regarding claim 11, Arimilli also discloses an input output unit coupled to the bus to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 12, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 13, Arimilli also discloses the bus is configured to transfer an entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 16, Arimilli also discloses support of a symmetric multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 18, Arimilli also discloses the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit (e.g., col. 7, lines 54-56).

6. *Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of Arimilli-2.*

Regarding claim 14, Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time the invention was made to obtain the claimed invention.

7. *Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of the standard practice of memory implementation, as further evidenced by Miller.*

Regarding claim 15, Arimilli fails to disclose the detail of using DRAM to implement memory; however the examiner takes Official Notice that the use of a

DRAM core is standard embodiment of a RAM memory. This is further evidenced by Miller. Miller discloses the embedded DRAM core (e.g., col. 5, lines 7-10). It would be obvious to combine standard implementation practice with Arimilli because the DRAM is a standard means to implement an embedded RAM core. Therefore it would be obvious to one of ordinary skill in the art to combine a standard memory embodiment with the disclosure of Arimilli and the well-known practice of integration.

8. *Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of a standard processor embodiment, as evidenced by Miller.*

Regarding claim 17, Arimilli neglects to disclose implementational details of a particular processor core; however the Examiner takes Official Notice that MIPS architecture is a standard processor for symmetric multiprocessing, such as in the system of Arimilli. This is further evidenced by Bitar. Bitar discloses the processor units are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line 39; and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious to combine Arimilli with the standard MIPS architecture, because the use of MIPS architecture is standard in the implementation of symmetric multiprocessing systems such as the system of Arimilli. Therefore at the time the invention was made, it would be obvious to a person of ordinary skill in the art to combine the MIPS architecture, a

standard embodiment as evidenced by Bitar, with Arimilli and the standard practice of integration to obtain the claimed invention.

9. *Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli, in view of standard practice of integration and memory implementation, as evidenced by Sherburne, and further in view of Arimilli-2.*

Regarding claim 19, Arimilli discloses and a power supply, a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the processor units; an embedded RAM core unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM core unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM core unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die and said invention occurring in a portable hand-held device; however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power consumption, and so forth. Likewise, the Examiner also takes Official Notice that the use of DRAM as a memory implementation is standard practice. This also is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices rendering the advantages of decreased size and weight (e.g., paragraph [0002]) as well as the manifest advantages of portability in a use such

as handheld device (e.g., paragraph [0002]) and also the use of DRAM to implement memory (e.g., Figure 1). It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which include multiprocessing systems with cache and embedded memory. Likewise the use of DRAM to implement memory as, evidenced by Sherburne, is standard practice. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not necessarily need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time the invention was made to obtain the claimed invention.

Regarding claim 20, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

(10) Response to Argument

Regarding claims 1-4, 7, and 9, Appellant argues that in Arimilli "snooping is performed by the storage device (or the internal processors thereof) and third party transactors" (p. 11); however it is not clear how this observation distinguishes Arimilli, where the internal processors, in the Appellant's words, anticipate the processors claimed. Furthermore, the "third party transactor" is the role the processor plays as a snooping device when a data transaction occurs on the bus that pertains to it; hence the entire point of snooping. Appellant further argues that "there is no teaching or suggestion that the snooping is for ensuring cache coherency between cache units"; however as cited supra, "if a match is found at step 610, the process continues at step 618 with the snoop device writing the target data into its memory" (col. 9, lines 43-45). This citation clearly shows that the bus is "configured to provide cache coherent snooping commands from the processor units" as claimed, and it clearly shows that it is "enables the processor units themselves to ensure cache coherency between the cache units" as claimed.

Appellant further alleges "an incredible degree of hindsight has been employed in combining the numerous cited references for the purpose of rejecting Appellant's Claims as proper motivation to combine the cited references is lacking (p. 12); however, inasmuch as this argument pertains to "the rejection of Claims 1-4, 7 and 9 under 35 U.S.C. §102(e)" (p. 10), there are no additional references used in the references; hence the credibility of the rejection relies on a single reference.

Regarding claim 5, Appellant argues that Arimilli (US 6,571,322) "does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that remedies the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above" (p. 13); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claim 6, Appellant argues that Miller "does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above" (p. 15); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claim 8, Appellant argues that Bitar "does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above" (p. 17); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claims 10-13, 16, and 18, Appellant argues that Sherburne "does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above" (p. 19); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claim 14, Appellant argues that Arimilli (US 6,571,322) "does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that remedies the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above" (p. 21); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claim 15, Appellant argues that Miller "does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above" (p. 23); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claim 17, Appellant argues that Miller "does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above" (p. 25); however the alleged deficiencies of Arimilli have been treated supra.

Regarding claims 19-20, Appellant argues that Arimilli (US 6,571,322) "does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) and Sherburne (U.S. Patent Application Publication No. 2002/0184546) that remedies the deficiencies of Arimilli et al. outlined above" (p. 28); however the alleged deficiencies of Arimilli have been treated supra.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Clifford Knoll

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